REMARKS

This paper is being provided in response to the Office Action mailed December 19, 2003, for the above-referenced application. In this response, Applicant has amended claims 4 and 8 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims are fully supported by the originally-filed specification.

Applicant thanks the Examiner for the indication of allowable subject matter in claim 8. Applicant has rewritten claim 8 into independent form to incorporate the base claim and any intervening claims and respectfully submits that this claim is in condition for allowance.

The rejection of claim 4 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,145,117 to Eng (hereinafter "Eng") in view of U.S. Patent No. 5,923,060 to Gheewala (hereinafter "Gheewala") and further in view of U.S. Patent App. Publication No. US 2003/0014201 to Schultz (hereinafter "Schultz") is hereby traversed and reconsideration is respectfully requested in view of the amendment to the claim contained herein.

Independent claim 4, as amended herein, recites a standard cell placement and routing processing system. The system includes a library file which stores information of various standard cells. Each standard cell includes a power supply terminal of a diffused layer, an input terminal of a first level metal and an output terminal of the first level metal. A circuit connection information file stores circuit connection information of an LSI to be developed. A constraint information file stores contained information concerning the placement and the routing. A parameter file stores parameter information including a power supply voltage and an operating

frequency of the LSI to be developed and a sheet resistance of the diffused layer. A placement and routing system executes the placement and the routing of standard cells selected in accordance with the circuit connection information from the circuit connection information file by utilizing information from the library file, the constraint information file and the parameter file. An input/output and display apparatus displays a history and a result of the placement and the routing and externally inputs a control command to control the placement and routing system. Further, the placement and routing system detects a signal line which becomes a hindrance in reducing the resistance of a power supply line, removes the signal line, and locates a connection path between the first level metal and a second level metal at an end position to which the removed signal line was connected.

The Eng reference discloses an electronic design automation system that provides for optimization of Register-Transfer-Level models of electronic designs. The system includes the generation of performance data for a variety of physical implementations to create a fully characterized library of logic building blocks. A high level chip optimization process can induce repartition to move logic between partitions, combine or split partitions as needed to meet design goals and generate timing and other constraints. A user interface device allows analyzing and probing of the electronic design by a designer. (See Abstract, col. 4, lines 21-65 and Figure 2 of Eng).

The Gheewala reference discloses a reduced area gate array cell design based on shifted placement of alternate rows of cells. The Office Action cites Gheewala as disclosing a gate array basic cell having power supply traces extending across diffusion regions, where power supply

traces are conductive bus regions coupled to the power supply source for the integrated circuit. (See col. 3, line 66 to col. 4, line 11 and Figure 4 of Gheewala).

The Schultz reference discloses a method for analyzing electromigration and voltage drop effects in wire segments of an integrated circuit. The Office Action cites Schultz as disclosing the use of the sheet resistance of a wire segment in designing a floor plan schematic of an integrated circuit. (See paragraphs 0082 and 0083 of Schultz).

Applicant's independent claim 4, as amended herein, recites at least the feature of a standard cell placement and routing processing system having a placement and routing system that *detects a signal line which becomes a hindrance in reducing the resistance of a power supply line, removes said signal line, and locates a connection path between said first level metal and a second level metal at an end position to which the removed signal line was connected.* (See, for example, page 25, lines 16 – page 26, line 20 and Figs. 12, 13A-13D, and 14 of the present application.) Applicant has found that with a system according to the present invention, it is possible to place and route standard cells having different widths with no hindrance, and it is also possible to set the width of the power supply line to an appropriate width for each standard cell array, resulting in the realization of a high wiring density. (See, for example, page 29, lines 1-7 of the present application.)

Applicant respectfully submits that neither Eng, Gheewala, nor Schultz, taken alone or in any combination, teach or fairly suggest at least the above-noted features as claimed by Applicant. Specifically, nothing in the prior art of record discloses a standard cell placement and

routing processing system having a placement and routing system that *detects a signal line which becomes a hindrance in reducing the resistance of a power supply line, removes said signal line, and locates a connection path between said first level metal and a second level metal at an end position to which the removed signal line was connected.* Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 5-7 and 9 under 35 U.S.C. 103(a) as being unpatentable over Eng in view of Gheewala and Schultz and further in view of U.S. Patent No. 6,405,346 to Nawa (hereinafter "Nawa") is hereby traversed and reconsideration is respectfully requested.

Submitted herewith is a verified translation of Japanese Patent Application No. 11-182445 (hereinafter "the Japanese Priority Application"), upon which the above-referenced U.S. patent application claims priority. The Japanese Priority Application was filed on June 28, 1999, and supports the claims of the present U.S. patent application, including claims 4-9. (See, for example, pages 1-7, pages 29-31 and Figs. 12-14 of the verified translation of the Japanese Priority Application). Accordingly, Applicant respectfully submits that the verified translation of the Japanese Priority Application entitles the above-referenced application to the filing date of the Japanese Priority Application, June 28, 1999.

With respect to the Nawa reference cited in the Office Action, Applicant respectfully submits that the date of the Japanese Priority Application, June 28, 1999, is prior to the December 29, 1999, filing date of the Nawa reference. Accordingly, Applicant respectfully

requests that the Nawa reference be withdrawn and that the rejection of the claims in view of the Nawa reference also be withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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